

00862.022499.



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
: Examiner: T. Nguyen
TAKAO YONEHARA, ET AL.)
: Group Art Unit: 2813
Application No.: 10/059,171)
: Filed: January 31, 2002)
: For: METHOD OF)
MANUFACTURING A)
THIN-FILM)
SEMICONDUCTOR DEVICE)
USED FOR A DISPLAY)
REGION AND PERIPHERAL)
CIRCUIT REGION) January 21, 2005

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

LETTER SUBMITTING PAPERS FOR PLACEMENT IN FILE

Sir:

Submitted herewith is a copy of a Search Report dated November 29, 2004, which issued in a European application corresponding to Application No. 10/687,743, together with copies of six documents cited therein (U.S. Patent Nos. 5,597,766, 5,888,882, and 6,017,804; WO 93/21663; Japan 55-145354; and EP 0 603 973). Also submitted herewith is a copy of an Office Action which issued in Application No. 10/059,144, together with copies of two documents cited therein (U.S. Patent No. 5,158,818 and Japan 11-317509). Applicants request that these papers be placed in the

Patent and Trademark Office file of the present application for the convenience of the public.

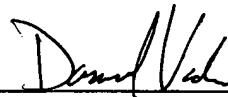
Japan 11-317509 is believed to be in the same patent family as U.S. Patent No. 6,342,433, which was previously cited in the subject application.

Japan 9-312349, which is listed in the European Search Report, and U.S. Patent No. 6,342,433, which is cited in the Office Action, are already of record in the subject application. Accordingly, copies of these documents are not enclosed.

This is not a request for consideration of the enclosed papers by the Examiner, and therefore, no Form PTO-1449 is submitted herewith nor is any fee or statement under 37 C.F.R. § 1.97 (e) believed to be required.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



Damond E. Vadnais
Attorney for Applicants
Registration No.: 52,310

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3800
Facsimile: (212) 218-2200

Notice of References Cited

Application/Control No.

10/059,144

Applicant(s)/Patent Under
Reexamination
YONEHARA ET AL.

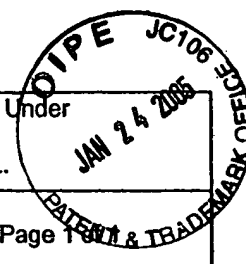
Examiner

Brook Kebede

Art Unit

2823

Page 1 of 1



U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,158,818	10-1992	Aurichio, Joseph A.	428/40.7
X	B	US-6,342,433	01-2002	Ohmi et al.	438/455
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
X	N	JP 11317509 A	11-1999	Japan	OHMI et al.	H01L 21/00
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22304-1450
www.uspto.gov

DEC 20 2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,144	01/31/2002	Takao Inehara	00862.022498	5995

5514 7590 12/15/2004

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER

KEBEDE, BROOK

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 12/15/2004



Please find below and/or attached an Office communication concerning this application or proceeding.

FILE NO. 00862.022498
ATTORNEY JSV
DUE DATE 3/15/05
DOCKETED 12/20/04
1/10/04

Office Action Summary

Application No.

10/059,144

Applicant(s)

YONEHARA ET AL.

Examiner

Brook Kebede

Art Unit

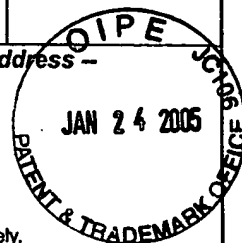
2823

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).



Status

- 1) ☒ Responsive to communication(s) filed on 22 November 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6, 8-10 and 13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 10 and 13 is/are rejected.
- 7) ☒ Claim(s) 8 and 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/22/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 22, 2004 has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-6, 10, and 13 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 6,677,183 in view of Omi et al. JP/11-317509, and further in view of Aurichio (US/5,158,818).

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

Re claim 1, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. The limitations

Art Unit: 2823

include a method of manufacturing a thin-film semiconductor device, comprising: the step of preparing a member having a semiconductor film with a semiconductor element semiconductor integrated circuit on a separation layer on which the semiconductor film is disposed (see Claim 1, lines 1-5); the separation step of separating the member at the separation layer by a pressure of a fluid (see Claim 1, lines 8-13); and the chip forming step after the separation step, forming the semiconductor film into chips (see Claim 15, lines 1-2).

However, the limitation "applying a pressure of a fluid to side surface of the separation layer" is not particularly is claimed in U.S. Patent No. 6,677,183.

Omi et al. (JP/11-317509) disclose applying a pressure fluid, such as water jet, to the side surface of separation layer in order to separate the layers of the device without damaging the surface (see the English translation that provided by the Office in Paragraph [0081] to [0084]).

Both U.S. Patent 6,677,183, in the claimed limitation, and Omi et al. (JP/11-317509) teachings are directed to bonding the semiconductor member and separating. Therefore, the claims of U.S. Patent 6,677,183 and the teaching Omi et al. (JP/11-317509) are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide U.S. Patent 6,677,183 with applying a pressure of a fluid to side surface of the separation layer as taught by Omi et al. (JP/11-317509) in order to separate the layers of the device without damaging the surface.

Although it is well-known in the art, the combination of U.S. Patent No. 6,677,183 as claimed and Omi et al. JP/11-317509 do not specifically disclose the use of adhesive during the bonding step of bonding member to a support member.

Aurichio discloses the use of conductive die attachment (i.e., an adhesive tape) in order to allow the mounting of the dice chip (i.e., a support member) to chip carrier (i.e., support). See Abstract.

U.S. Patent 6,677,183, in the claimed limitation, Omi et al. (JP/11-317509), and Aurichio (US/5,158,818).

teachings are directed to bonding the semiconductor member and separating. Therefore, the claims of U.S. Patent 6,677,183 and the teaching Omi et al. (JP/11-317509) are analogous. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide U.S. Patent 6,677,183 and Omi et al. (JP/11-317509) with bonding step of bonding the member to support member via an adhesive as taught by Aurichio in order to allow the mounting of the dice chip (i.e., a support member) to chip carrier (i.e., support).

Re claim 2, as applied to claim 1 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. In addition, the limitations wherein the member is obtained by forming a porous layer on a surface of a semiconductor substrate, forming the semiconductor film on a surface of the porous layer, and then forming the semiconductor element and/or semiconductor integrated circuit is claimed in Claim 3 of U.S. Patent No. 6,677,183 (see Claim 3, lines 1-5).

Re claim 3, as applied to claims 1 and 2 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 3, and 15 of U.S. Patent No. 6,677,183. Further the limitation, wherein the semiconductor film is formed on the surface of the porous layer after forming a protective film on inner walls of pores in the porous layer is claimed in Claim 4 of U.S. Patent No. 6,677,183 (see Claim 4, lines 1-6).

Re claim 4, as applied to claim 1 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. Furthermore, the limitation, wherein the member is obtained by forming the semiconductor element and/or semiconductor integrated circuit on a surface of a semiconductor substrate and implanting ions from the surface side to a predetermined depth to form the separation layer is claimed in Claim 18 of U.S. Patent No. 6,677,183 (see Claim 18, lines 12-16).

Re claim 5, as applied to claims 1 and 2 above the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 3, and 15 of U.S. Patent No. 6,677,183. Further the limitation, wherein the semiconductor substrate is a single-crystal silicon substrate or a compound semiconductor substrate is claimed in Claim 5 of U.S. Patent No. 6,677,183 (see Claim 5, lines 1-3).

Re claim 6, as applied to claims 1 and 4 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 15 and 18 of U.S. Patent No. 6,677,183. In addition, the limitation wherein the semiconductor substrate is a single-crystal silicon substrate or a compound semiconductor substrate is claimed in Claim 5 of U.S. Patent No. 6,677,183 (see Claim 5, lines 1-3).

Re claims 10 and 13 the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. The limitations include a method of manufacturing a thin-film semiconductor device, comprising: the step of preparing a member having a semiconductor film with a semiconductor element and/or semiconductor integrated circuit on a separation layer on which the semiconductor disposed (see Claim 1, lines 8-13); the chip forming step of forming the member

Art Unit: 2823

into chips in desired regions; and the separation step of, after the chip forming step, separating the member at the separation layer (see Claim 15, lines 1-2).

However, the limitation "a bonding step of bonding the member to support member" is not particularly is claimed in U.S. Patent No. 6,677,183.

Omi et al. (JP/11-317509) a bonding step of bonding the member to support member (see Drawing 8) in order bonded semiconductor base substrate or another composite member, so that separation does not occur before the separation process, and separation is securely performed in the separation process.

Both U.S. Patent 6,677,183, in the claimed limitation, and Omi et al. (JP/11-317509) teachings are directed to bonding the semiconductor member and separating. Therefore, the claims of U.S. Patent 6,677,183 and the teaching Omi et al. (JP/11-317509) are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide U.S. Patent 6,677,183 with a bonding step of bonding the member to support member as taught by Omi et al. (JP/11-317509) in order to separate the layers of the device without damaging the surface.

Although it is well-known in the art, the combination of U.S. Patent No. 6,677,183 as claimed and Omi et al. JP/11-317509 do not specifically disclose the use of adhesive during the bonding step of bonding member to a support member.

Aurichio discloses the use of conductive die attach (i.e., an adhesive tape) in order to allow the mounting of the dice chip (i.e., a support member) to chip carrier (i.e., support). See Abstract.

U.S. Patent 6,677,183, in the claimed limitation, Omi et al. (JP/11-317509), and Aurichio (US/5,158,818).

Art Unit: 2823

teachings are directed to bonding the semiconductor member and separating. Therefore, the claims of U.S. Patent 6,677,183 and the teaching Omi et al. (JP/11-317509) are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide U.S. Patent 6,677,183 and Omi et al. (JP/11-317509) with bonding step of bonding the member to support member via an adhesive as taught by Aurichio in order to allow the mounting of the dice chip (i.e., a support member) to chip carrier (i.e., support).

Therefore, the conflicting claims are not patentably distinct from each other.

Allowable Subject Matter

4. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicants' arguments with respect to claims 1-6, 10, and 13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

Art Unit: 2823

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

BK
December 13, 2004

Brook Kebede